High voltage module with low internal inductance for next chip generation - next High Power Density Dual ($_nHPD^2$) -

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Abstract

In order to obtain the full benefit of Wide Band Gap (WBG) semiconductor device, it is essential to reduce total system stray inductance. Hitachi's latest package technology development is the new high voltage package concept named "next High Power Density Dual ($_nHPD^2$)". The package offers not only a drastic reduction in the internal inductance by 75% from conventional modules, but also an increase in the power density compared with the latest F-version series modules. Hitachi formerly presented the latest generation F-series modules in 2014, showing a 20% higher power density compared to conventional devices in the market. $_nHPD^2$ provides even higher power densities, up to 10% more. The developed package is equipped with a current sensing function which enables the user to detect the voltage difference using the internal package inductance. Although it is challenging to apply the current sensing method using the internal inductance with high accuracy in spite of the extremely low inductance module, in this paper we propose a new current sensing algorism using the internal inductance and verified to show adequate accuracy.

1. Introduction

WBG semiconductor technology offers very low switching characteristics, not only for high frequency DC-DC conversion, but also for motor control [1]. However, when it is applied to the motor control system, the switching oscillation will be the inevitable problem. In order to

avoid this problem, decrease in switching speed may be one of the countermeasures, but that unfortunately negates the benefit of the WBG device. Reduction of inductance is another more viable solution. This approach has been reported by many researchers [2], [3], [4]. In Fig.1, the relationship between switching loss and loop inductance is presented. The gate resistance (Rg) in this figure represents the parameter of switching speed. In this paper, we have defined the internal inductance target as 10nH.

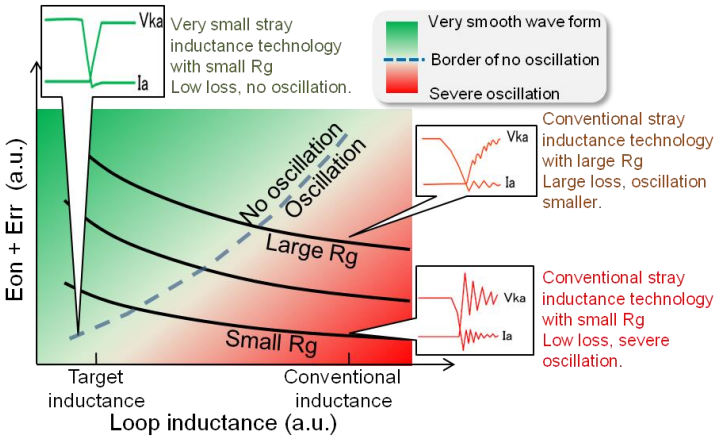
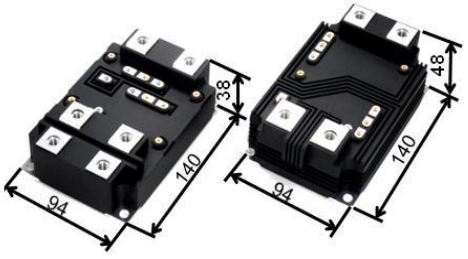


Fig.1 System loop inductance & gate resistor trade-off

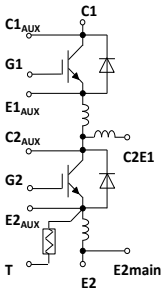
2. Low internal inductance package

2.1. Package series

Fig.2 shows the package outline corresponding to circuit diagram and rated voltage and current of Hitachi's new package, $_{n}$HPD^{2}. A single common foot-print size covers a wide range of use from 1200V to 6500V. Here, LV and HV packages are defined for each voltage level. LV and HV have an isolation voltage of 6.0kVrms and 10.2kVrms respectively. As shown in circuit diagram, $_{n}$HPD^{2} consists of a dual switch to achieve low internal inductance. We installed a current sensor utilizing stray inductance. In this paper, the electric characteristics of the LV package are reported.



a) LV package b) HV package



c) Circuit diagram

Package	Vces	Ic
LV	1200V	1000A
LV	1700V	900A
LV/HV	3300V	450A
HV	4500V	330A
HV	6500V	225A

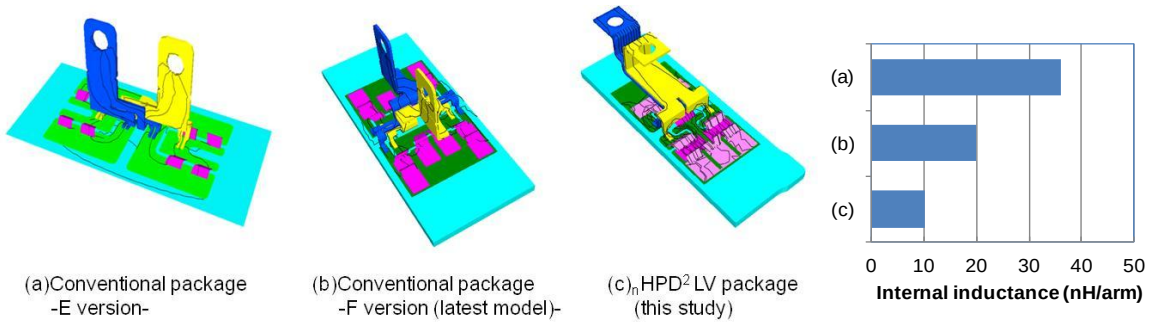
d) Rated voltage and current

Fig. 2 Package outline and circuit diagram of $_{n}$HPD^{2}, covering voltage and current

2.2. Optimizing terminal design

As for optimizing terminal design within the module, we should consider not only lowing the inductance but also mechanical stress and temperature rise. With regard to the inductance reduction, it is worthwhile to utilize the mutual inductance between anti-parallel terminals. Our

latest package, F-version, shown in Fig.3(b) achieved a reduction of the stray inductance by approximately 40% compared to conventional packaged, E-version shown in Fig.3(a), by arranging most of area of terminal face-to-face with a short distance [5],[6]. Furthermore, by enlarging the area of terminals with a dual switching circuit, our new model, $_{n}HPD^{2}$, managed to decrease the inductance even lower, as shown in Fig.3(c). Fig. 4 showed comparisons of turn-off waveform between the conventional package and $_{n}HPD^{2}$. Due to low internal inductance, $_{n}HPD^{2}$ demonstrated a smaller turn-off peak voltage. Internal inductance was evaluated as 9.7nH, which fulfilled our target value for WBG device applications.

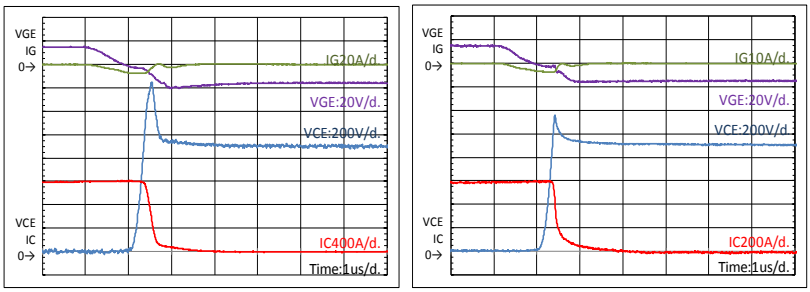


(a)Conventional package -E version-

(b)Conventional package -F version (latest model)-

(c)$_{n}HPD^{2}$ LV package (this study)

Fig.3 Electro-magnetic analysis and measurement of internal inductance



(a) Conventional package 1200A/1700V dual

condition:Vcc=900V, Ic=1200A, Tj=125℃
Vge=+15/-15V, Rg=1.5Ω, Cge=120nF
Ls=100nH

(b) $_{n}HPD^{2}$

condition:Vcc=900V, Ic=600A, Tj=125℃
Vge=+15/-15V, Rg=3.3Ω, Cge=60nF
Ls=20nH

Fig. 4 Comparison of turn-off wave form: $_{n}HPD^{2}$ and conventional package

3. Advantages from inverter perspective

3.1. Dual switch concept (low inductance)

The dual-switch concept was an important condition to realize the 75%-reduction of each phase leg. The inductances of single phase configured $_{n}HPD^{2}$ modules were compared. See Fig. 5. The left side illustration shows two single switch packaged configuration, rated at either 800A or 1200A with the stray inductance of 18nH (or 10nH for latest 1200A F-version). As a phase leg, the total phase inductance was estimated as 36nH. The illustration on the right side is $_{n}HPD^{2}$ dual switch configuration with a stray inductance of 10nH. The equivalent

inductance of the total phase was only 5nH (10nH/2). This means $_{n}$HPD^{2} offered a drastic reduction in the internal inductance by 75% from conventional module. Fig.5 also depicted the relative power densities based on the occupied area size and the rated current for 3 phase leg. From this figure, we verified that $_{n}$HPD^{2} improved power density by 10% when compared to our latest conventional module which increased power density by 20% in 2014[5],[6].

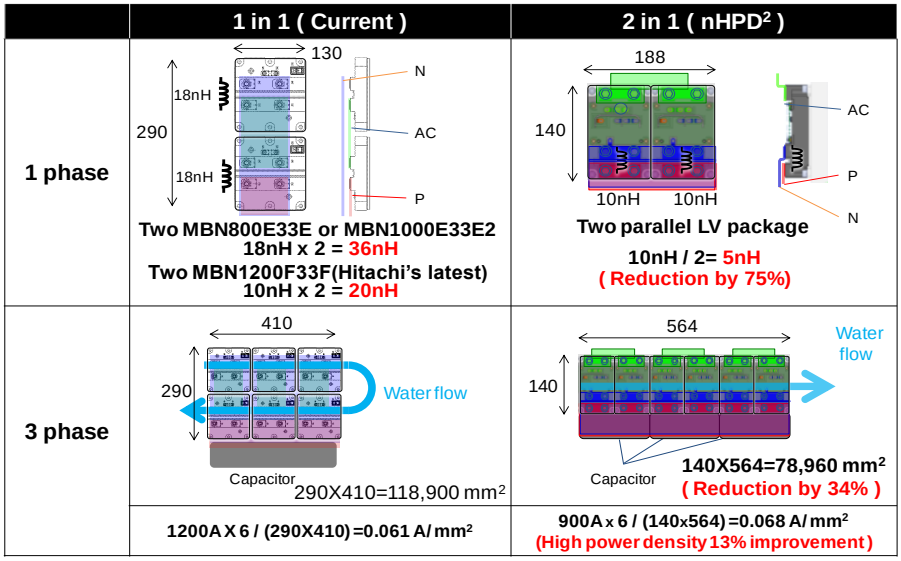


Fig. 5 Converter layout comparison between conventional package and $_{n}$HPD^{2}

3.2. Parallel use of $_{n}$HPD^{2} (Higher output)

Featuring a P and N terminal pair on one of the short sides and the AC terminal at the opposite side, nHPD2 provided building-block assembly design concept. Connection to sub-systems and components was made simpler by separating DC and AC lines. This enabled smaller inverter designs by optimal DC-link capacitor and load connections. Fig.6 shows an example of the assembled layout in case of nHPD2 with two modules in parallel and a 3-phase configuration (6 $_{n}$HPD^{2} used in total). In case of parallel use, it is prudent to consider about any possible imbalance between modules. On the DC terminal side, capacitors were equally implemented to each $_{n}$HPD^{2} in order to prevent imbalance. On the other hand, along the AC terminal side, a common busbar was connected to two $_{n}$HPD^{2} modules. Here, we should consider the inductance of the AC busbar because the internal inductance of $_{n}$HPD^{2} is relatively small. It is especially important to consider the stray inductance of the AC terminal to take into account and prevent any potential imbalance. Fig.7 highlights the short circuit current of two (2) parallel connected $_{n}$HPD^{2} modules. As a direct consequence of the inductance balance, short circuit current balanced very well and no major waveform differences were observed.

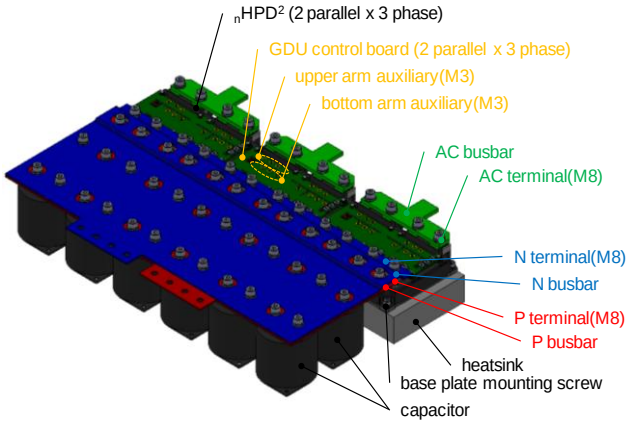
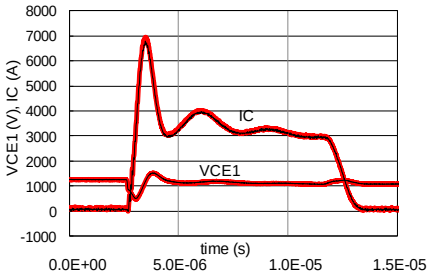


Fig. 6 An example of the assembled layout



condition: Vcc=1100V, RT, VGE=+15V/-15V,
Rg(on/off)=1.5Ω/15Ω, Cge=60nF,
15V back-to-back zenner diode
upper arm, 2 modules in paralell
red line and black line correspond to each module

Fig. 7 Short circuit type I waveform of 2 parallel connected $_nHPD^2$

4. Current sensing function

4.1. Current sensor for low inductance package

$_nHPD^2$ is low internal inductance package to prevent oscillation in case of WBG semiconductor implementation. Due to low internal inductance, turn-on loss was getting larger than conventional packages because the voltage difference at switching device was increased during turn-on period. This large turn-on loss is not acceptable, so in order to compensate turn-on loss, small gate resistance (Rg) should be selected to make di/dt larger. Small Rg make di/dt larger right after the short circuit, as well. Thus, the low inductance package was suitable to detect short circuit current by detecting di/dt directly.

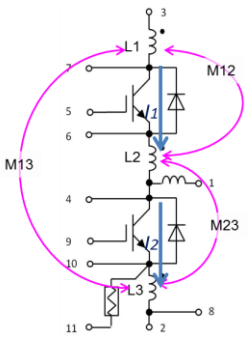
4.2. di/dt detection accuracy on low internal inductance package

Current sensing technology using internal inductances was reported [7]. In this technology larger inductance was required to retain enough accuracy. It contradicted the low loss characteristics of using low inductance packaging. In this paper, $_nHPD^2$ was equipped with current sensing terminal utilizing “internal” inductance whose value was relatively small. By referring to the conventional algorithm, the current of upper arm was detected from the potential difference (L2*dI1/dt) between auxiliary terminals 6 and 4 defined in Fig.5 circuit topology. For the bottom arm, terminals 10 and 8 were used to obtain the potential difference (L3*di2/dt). To realize the low inductance package, terminals were designed to make current flows in an anti-parallel direction at the small distance. Therefore, the mutual inductance between adjacent terminals cannot be ignored in this study. Now we propose the new algorithm to accurately estimate the collector current from the measured potential drop (V6-4 and V10-8) described as eq.(1). This equation can be converted to eq.(2) and the current in upper arm and bottom arm can be expressed as eq.(3). Using numerical electro-magnetic

analysis method, each lumped constant was also computed.

Fig. 9 showed the example of our experimental results of estimated current. Firstly, Type I short circuit waveforms were compared. Estimated currents by conventional methodology were less than half and more than twice for bottom and upper arm. According to this algorithm, estimated current fitted to measured current well.

Secondly, type II and type III short circuits were also evaluated. Using the same algorithm, Fig. 10 shows the estimated current and measured current of type II and type III short circuits. Both estimated currents fitted to the measured currents well.

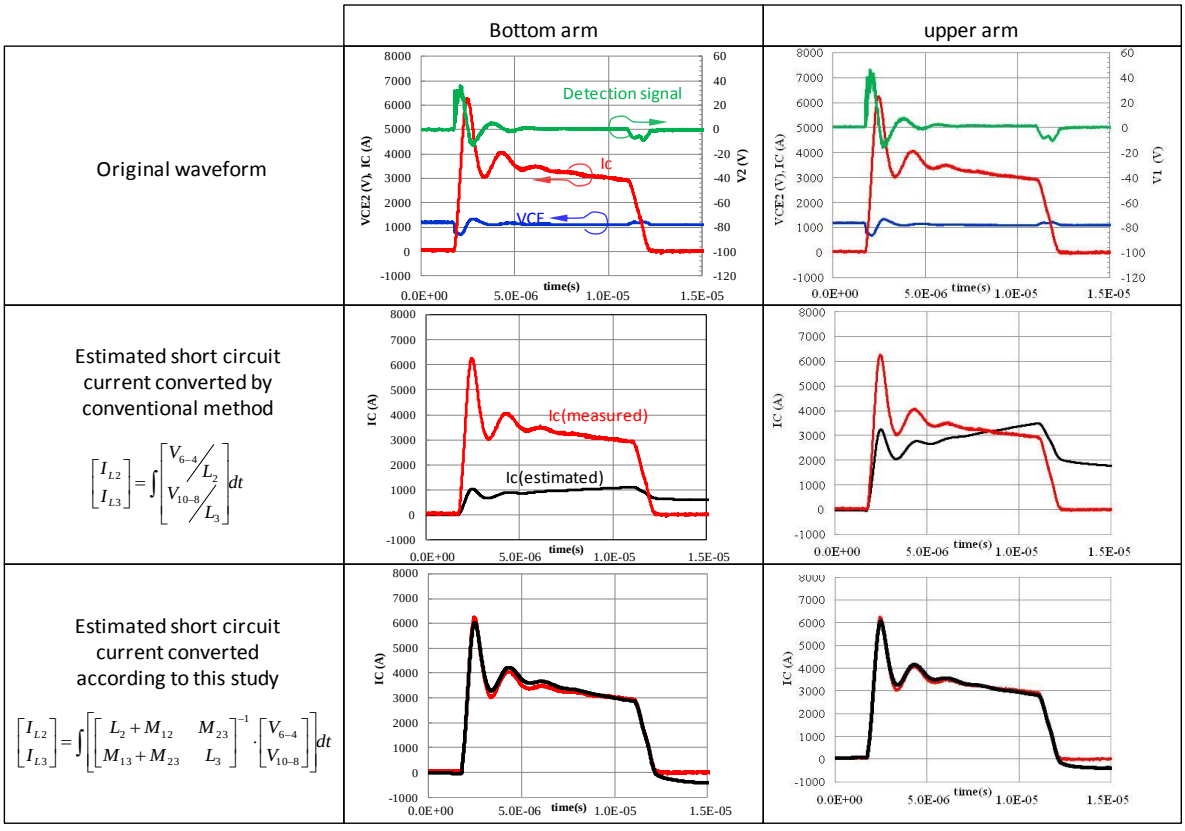


$$\begin{bmatrix} V_{6-4} \\ V_{10-8} \end{bmatrix} = \begin{bmatrix} L_2 + M_{12} & M_{23} \\ M_{13} + M_{23} & L_3 \end{bmatrix} \cdot \begin{bmatrix} \frac{dI_{L2}}{dt} \\ \frac{dI_{L3}}{dt} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} \frac{dI_{L2}}{dt} \\ \frac{dI_{L3}}{dt} \end{bmatrix} = \begin{bmatrix} L_2 + M_{12} & M_{23} \\ M_{13} + M_{23} & L_3 \end{bmatrix}^{-1} \cdot \begin{bmatrix} V_{6-4} \\ V_{10-8} \end{bmatrix} \quad (2)$$

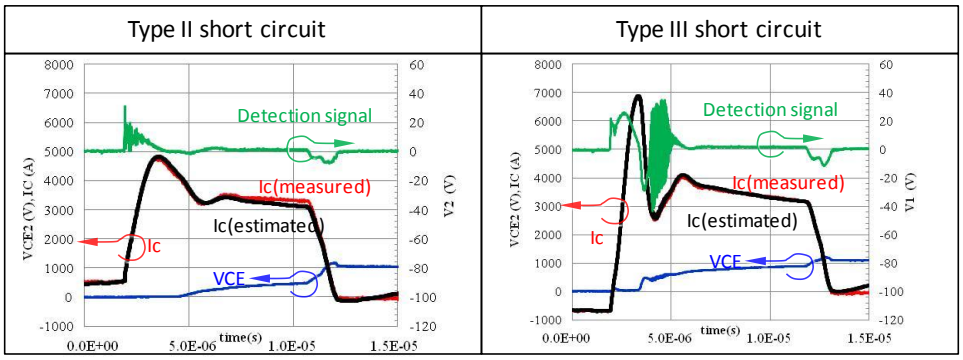
$$\begin{bmatrix} I_{L2} \\ I_{L3} \end{bmatrix} = \int \left[\begin{bmatrix} L_2 + M_{12} & M_{23} \\ M_{13} + M_{23} & L_3 \end{bmatrix}^{-1} \cdot \begin{bmatrix} V_{6-4} \\ V_{10-8} \end{bmatrix} \right] dt \quad (3)$$

Fig.8 Circuit topology of $_nHPD^2$ and proposed current sensing algorithm



condition: Vcc=1100V, RT, VGE=+15V/-15V,Rg(on/off)=3Ω/33Ω, 15V back-to-back zenner diode

Fig. 9 Waveforms of type I short circuit, detected voltage, and estimated collector current comparing conventional method and proposed method



condition:
Vcc=1100V, RT,
VGE=+15V/-15V,
Rg(on/off)=3Ω/33Ω,
15V back-to-back
zenner diode

Fig. 10 Comparison with short circuit current and estimated current by di/dt detection

5. Conclusions

We have developed the next high power density dual ($_n$HPD^2) package, which has a low internal inductance of less than 10nH. Since $_n$HPD^2 was designed as a dual switch configuraion, it offered a drastic reduction in the internal inductance of the total phase by 75% from conventional module. We also verified that $_n$HPD^2 improved the power density by 10% versus our latest inductance modules. We proposed the new algorithm using the module internal inductance in order to estimate the collector current from measured voltage drop. The new method utilized the mutual inductance between adjacent terminals and was considered to offer a high degree of accuracy.

The predicted collector current value using our proposed algorithm were fitted to the experimental results very well in spite of the extremelly low inductance module.

6. Reference

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