3-Phase IGBT/MOS Gate Driver IC
ECN33550FP Product Specifications Rev.0

1. Product Description

1.1 Features

(1) A motor is driven by three input signals (UI, VI, WI)

(2) Dead time and six control signals from three input signals are generated

(3) Free run condition is detected by the built-in back EMF* detection circuit

(4) Maximum Ratings: 620V, suitable for the system from 200VAC to 240VAC

(5) Drives a motor using a high voltage DC power supply and a low voltage DC power supply (15V)

1.2 Functions

(1) Three input type

(2) Built-in dead-time generating function (Top and bottom arm short-circuit protection)

(3) FU and FV signal output pins for U and V-phase back EMF detection

(4) All off signal input pin

(5) Fault output pin

(6) Built-in bootstrap diode

(7) 5V power supply

(8) Over-current protection

(9) 15V_VCC low-voltage detection

(10) Top arm low-voltage detection

*EMF: Electromotive Force

1.3 Block Diagram

The ECN33550 is shown inside the bold line.

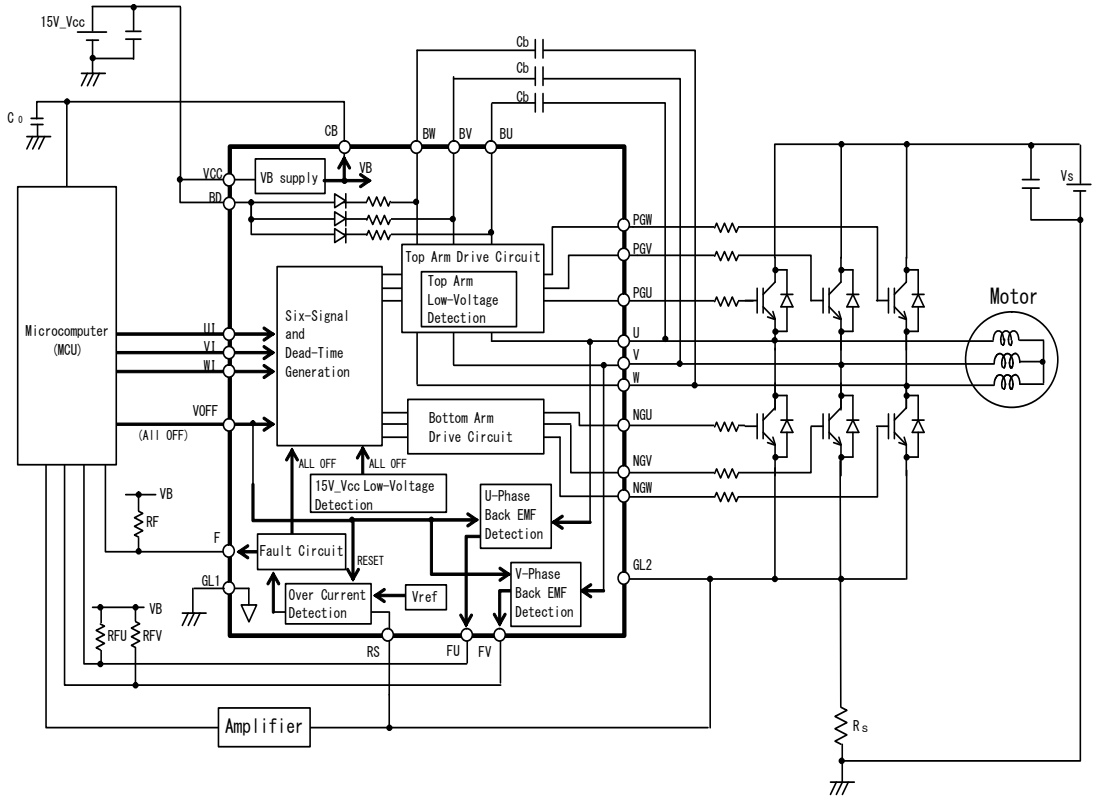
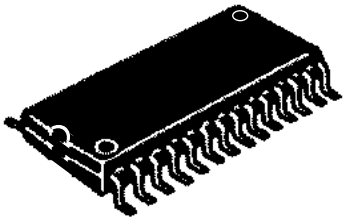


FIGURE 1.3.1 Block Diagram

1.4 Packages



ECN33550FP
(Package: SOP-28)

FIGURE 1.4.1 Packages of ECN33550FP

2. Specification

2.1 Maximum ratings

TABLE 2.1.1 Maximum ratings Condition: Ta=25℃

No.	Item	Symbol	Pin	Rating	Unit	Condition
1	High voltage device breakdown voltage	VBV	BU,BV,BW	620	V	
2	GL2 pin voltage	VGL2	GL2	-5 to VCC	V	
3	U, V, W pin voltage	VU,VV,VW	U,V,W	-5 to 600	V	
4	Voltage between BU-BD, BV-BD, BW-BD	VBUD VBVD VBWD	BU,BV,BW, BD	-5 to 600	V	
5	VCC power supply voltage	15V_VCC	VCC	20	V	
6	Voltage between BU-U, BV-V, BW-W	VBSU VBSV VBSW	BU,U BV,V BW,W	20	V	
7	Voltage between VCC-GL2	VCCGL2	VCC,GL2	23	V	-5V≦VGL2≦-3V
8	Input voltage	VIN	UI,VI,WI VOFF,RS	-0.5 to VB+0.5	V	
9	Fault pin voltage	Vflt	F	-0.5 to VB+0.5	V	
10	FU, FV pin voltage	Vfu,Vfv	FU,FV	-0.5 to VB+0.5	V	
11	VB supply output current	IBMAX	CB	50	mA	
12	Operating junction temperature	Tjop	—	-40 to +125	℃	
13	Storage temperature	Tstg	—	-40 to +150	℃	

Note 1: Thermal resistance
Between junction and air (Mounted PCB*) : 96℃/W [Reference value]
(Material of PCB : Glass epoxy, PCB size : 40mm×40mm×1.6mm, Wiring density : 10%)

*PCB: Printed Circuit Board

2.2 Electrical Characteristics

TABLE 2.2.1 Electrical Characteristics Suffix (T: Top arm, B: Bottom arm) Condition: Ta=25℃

No.	Item		Symbol	Pin	Min.	Typ.	Max.	Unit	Condition
1	Standby current		Is1	VCC	—	3	10	mA	VCC=15V, GL2=0V VOFF=0V, IB=0A
			Is2	BU,BV,BW	—	15	30	μA	Between BU-U,BV-V,BW-W=15V
2	Output source current		Io+	PGU,PGV,PGW NGU,NGV,NGW	0.20	0.25	—	A	VCC=15V, Pulse width≦10μs Between BU-PGU,BV-PGV, BW-PGW,VCC-NGU,NGV,NGW=15V
3	Output sink current		Io-	PGU,PGV,PGW NGU,NGV,NGW	0.30	0.40	—	A	VCC=15V, Pulse width≦10μs Between PGU-U,PGV-V,PGW-W, NGU,NGV,NGW-GL2=15V
4	High level output voltage		VOH	PGU,PGV,PGW NGU,NGV,NGW	—	—	100	mV	VCC=15V, Io+=0A Between BU-PGU,BV-PGV,BW-PGW Between VCC-NGU,NGV,NGW
5	Low level output voltage		VOL	PGU,PGV,PGW NGU,NGV,NGW	—	—	100	mV	VCC=15V, Io-=0A Between PGU-U,PGV-V,PGW-W Between NGU,NGV,NGW-GL2
6	Output delay time	Turn ON	TdONT	PGU,PGV,PGW	—	1.4	2.5	μs	VCC=15V, CL=1000pF
7			TdONB	NGU,NGV,NGW	—	1.4	2.5	μs	
8		Turn OFF	TdOFFT	PGU,PGV,PGW	—	0.4	1.0	μs	VCC=15V, CL=1000pF
9			TdOFFB	NGU,NGV,NGW	—	0.4	1.0	μs	
10	Dead-time	Top arm ON	TDT	PGU,PGV,PGW NGU,NGV,NGW	0.5	1.0	1.7	μs	VCC=15V, CL=1000pF NOTE 1
11		Bottom arm ON	TDB		0.5	1.0	1.7	μs	
12	Leakage current at high voltage pin		IL	BU,BV,BW U,V,W	—	—	10	μA	BU,BV,BW=U,V,W=450V
13	Over-current protection reference voltage		Vref	RS	0.45	0.50	0.55	V	VCC=15V
14	Over-current protection delay time		Tref	RS	—	2.0	4.0	μs	VCC=15V, CL=1000pF
15	UI,VI,WI, VOFF inputs	Voltage	VIH	UI,VI,WI, VOFF	2.5	—	—	V	VCC=15V
16			VIL		—	—	1.0	V	
17		Current	IIL	UI,VI,WI, VOFF	-10	—	—	μA	Input =0V, VCC=15V Pull-down resistor NOTE 2
18			IIH		—	—	100	μA	Input =4.5V, VCC=15V
19	RS input current		IILRS	RS	-100	—	—	μA	VCC=15V, RS=0V Pull-up resistor NOTE 3
20	VB supply output	Voltage	VB	CB	4.5	5.0	5.5	V	VCC=15V, IB=0A
21		Current	IB	CB	—	—	45	mA	VCC=15V
22	LVSD	Operating voltage	LVSDON	VCC	9.5	11.0	12.5	V	NOTE 4
23		Recovery voltage	LVSDOFF		10	11.5	13.0	V	
24	Top arm LVSD	Operating voltage	LVSDONT	BU,BV,BW	9.0	10.5	12.0	V	
25		Recovery voltage	LVSDOFFT		9.5	11.0	12.5	V	
26	F,FU,FV output resistance		RON	F,FU,FV	—	0.4	0.8	kΩ	I= -1mA NOTE 5
27	Fault reset delay time		tflrs	F	—	15	30	μs	VCC=15V
28	All off delay time		taoff	VOFF	—	0.3	2.0	μs	VCC=15V, CL=1000pF
29	Bootstrap diode forward voltage		VFDB	BU,BV,BW,BD	—	1.0	1.5	V	I=1mA, Between BD-BU,BV,BW Included series resistance
30	Back EMF detection level		VIHE	U,V	4	—	—	V	VCC=15V, VOFF=0V
31			VILE		—	—	1	V	

Note 1: FIGURE 2.4.2.1 shows definition of the dead-time. The values shown in No.10 and No.11 are based on the actual measured values of the ECN33550. They don't correspond to the values calculated from the values shown in No.6 to No.9.

Note 2: Internal pull-down resistor is typically 200kΩ. The equivalent circuit is shown in FIGURE 2.2.1.

Note 3: Internal pull-up resistor is typically 200kΩ. The equivalent circuit is shown in FIGURE 2.2.2.

Note 4: The LVSD function detects and shuts down at low VCC.

Note 5: The equivalent circuit is shown in FIGURE 2.2.3.

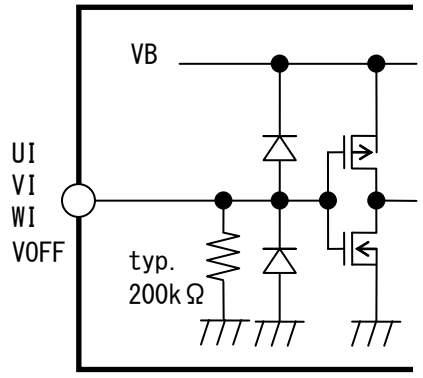


FIGURE 2.2.1 Equivalent Circuit around UI, VI, WI, VOFF Pins

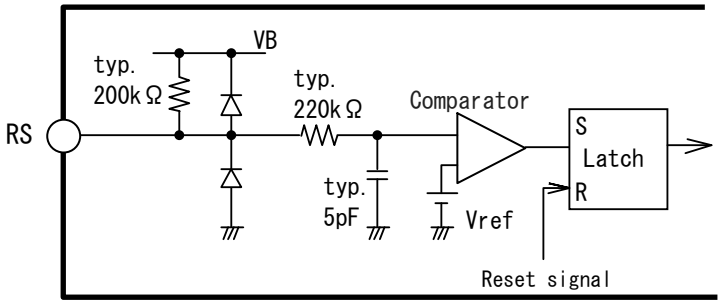


FIGURE 2.2.2 Equivalent Circuit around RS Pin

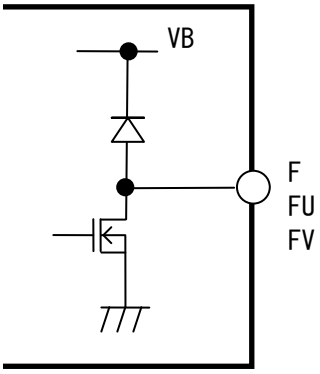


FIGURE 2.2.3 Equivalent Circuit around F, FU, FV Pins

2.3 Operating Condition

TABLE 2.3.1 Operating Condition Condition: Ta=25℃

No.	Item	Symbol	Pin	Min.	Typ.	Max.	Unit	Condition
1	U, V, W voltage	VUVWop	U, V, W	−3	-	450	V	VCC=15V Each voltage between BU-U, BV-V,BW-W: 15V
2	VCC voltage	VCCop	VCC	13.5	15	16.5	V	
3	Voltage between BU-U, BV-V, BW-W	VBSUop VBSVop VBSVop	BU, U BV, V BW, W	12.0	15	16.5	V	

2.4 Functions and Operations

2.4.1 Truth Table

TABLE 2.4.1.1 Truth Table

Pin	Input	Top arm output	Bottom arm output
UI, VI, WI	L	OFF	ON
	H	ON	OFF
VOFF	L	ALL OFF	
	H	Based on UI, VI, WI input	

2.4.2 Dead time

The ECN33550 generates six output signals with dead time from three input signals (UI, VI, WI).

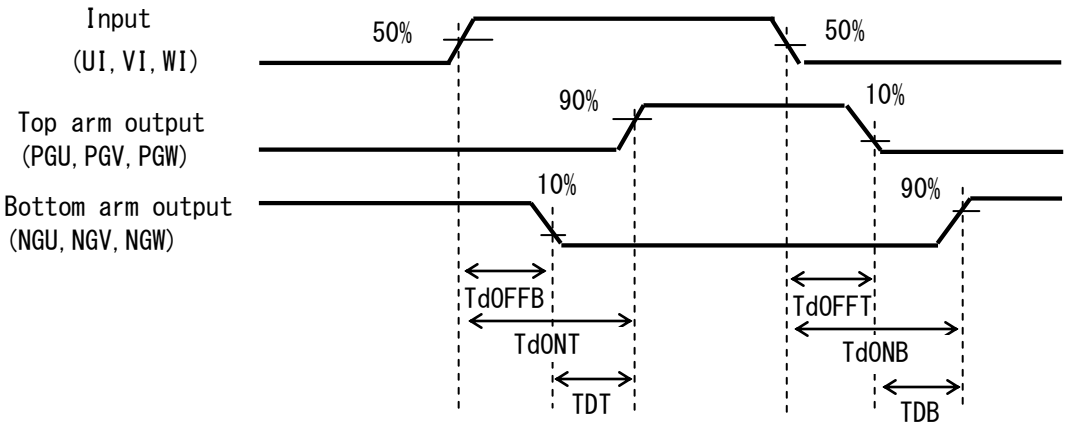


FIGURE 2.4.2.1 Definition of Dead time (Capacitive Load)

2.4.3 All Output Shutoff Function

When the “L” signal is input to the VOFF pin, the outputs of the top and bottom arms become all “L”.

When the “H” signal is input to the VOFF pin, the ECN33550 outputs the signals in accordance with TABLE 2.4.1.1.

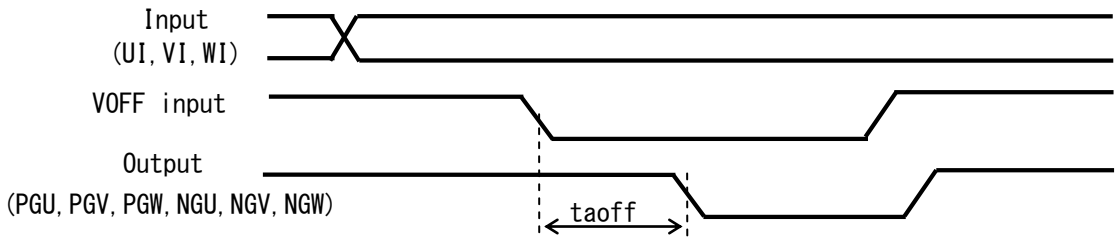


FIGURE 2.4.3.1 Definition of taoff

2.4.4 Over-Current Protection

The ECN33550 monitors the current through the shunt resistance Rs. When the voltage at the RS pin exceeds the Vref (Typ. 0.5V) of the internal detection circuit, the outputs of the top and bottom arms become all “L” and the F pin outputs “L”. Input “L” at the VOFF pin to reset this “All-Off” state. The F pin outputs “H” by inputting “L” after a lapse of the fault reset delay time (tflrs). Lengthen the period of the VOFF “L” for the fault reset delay time or more.

Just after the VCC power supply is turned on, the over current protection may operate. In this case, reset the “All-Off” state.

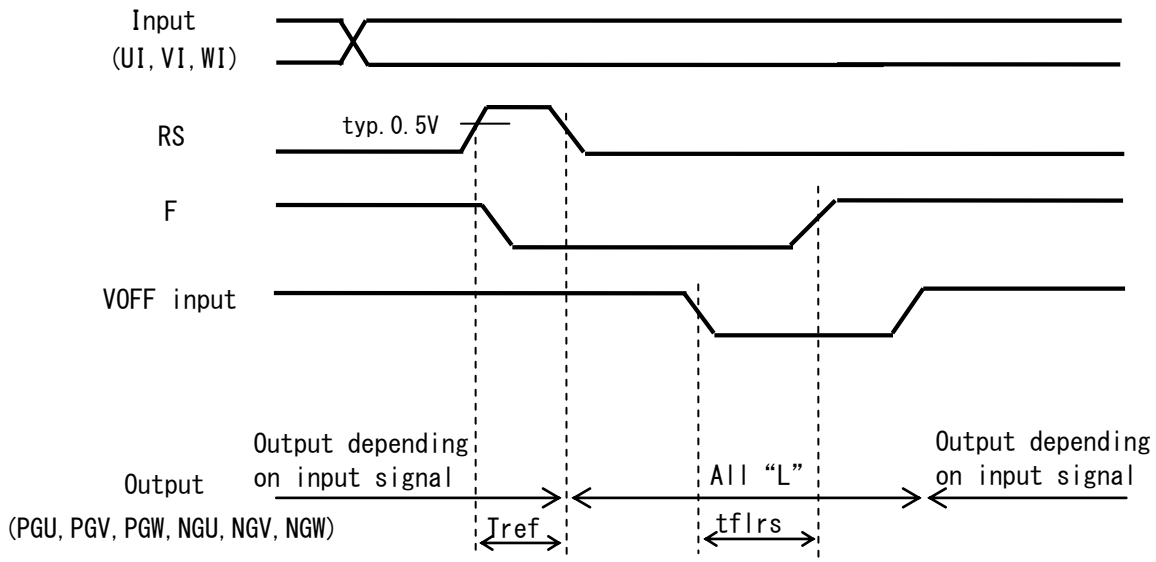


FIGURE 2.4.4.1 Definition of Tref and tflrs

2.4.5 15V_VCC Low-Voltage Detection

When the 15V_VCC voltage goes below the LVSD operating voltage (LVSDON), the outputs of the top and bottom arms become all “L”. When the 15V_VCC voltage goes up, this all “L” state is reset at the LVSD recovery voltage (LVSDOFF).

2.4.6 Top Arm Low-Voltage Detection

When the voltage between BU and U (BV and V, or BW and W) goes below the top arm low-voltage detection operating voltage (LVSDONT), the top arm output of the corresponding phase becomes “L”. The “L” output state is reset when the “H” signal is input to the top arm after the voltage between BU and U (BV and V, or BW and W) goes up to the top arm low-voltage detection recovery voltage (LVSDOFFT).

3. Standard Applications

3.1 External Components

TABLE 3.1.1 External Components

Component	Standard value	Usage	Remark
C0	1.0μF ± 20%	Smooths the internal power supply (VB)	Voltage stress is VB (=5.5V)
Cb	3.3μF ± 20%	For bootstrap	Voltage stress is 15V_VCC
Rs	Note 1	Sets over-current protection	
RF, RFU, RFV	10kΩ±5%	Pull-up resistor	

Note 1. The over-current detection setting IO is calculated as follows.
IO = Vref / Rs (A)

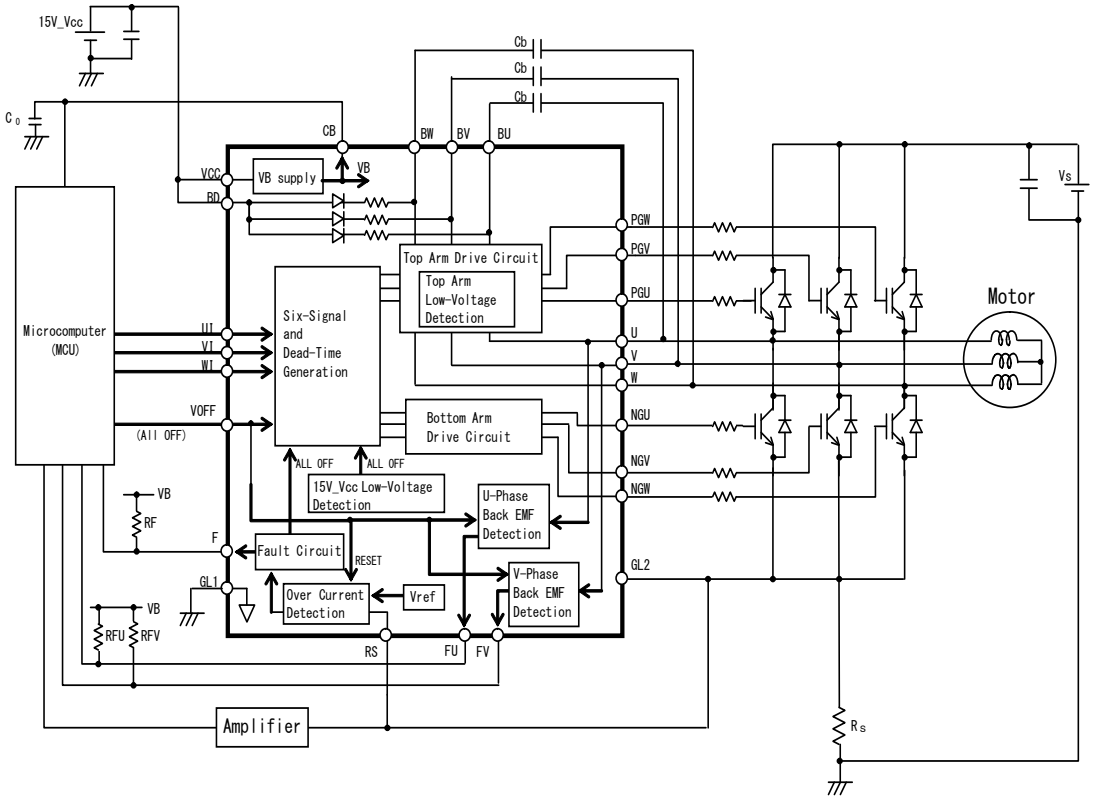


FIGURE 3.1.1 Block Diagram (ECN33550 is shown inside the bold line.)

3.2 Input Pins (UI, VI, WI, VOFF)

In some applications, input pins may be sensitive to noise due to high impedance. If noise is detected at an input pin, the following resistor and/or capacitor should be added.

- Resistor : 5.6kΩ ± 5% pull-down resistor between the GL pin and input pins
- Capacitor : 470pF ± 20% ceramic capacitor close to the input pins (UI, VI, WI)
  0.01μF ± 20% ceramic capacitor close to the input pin (VOFF)

4. Pin Locations

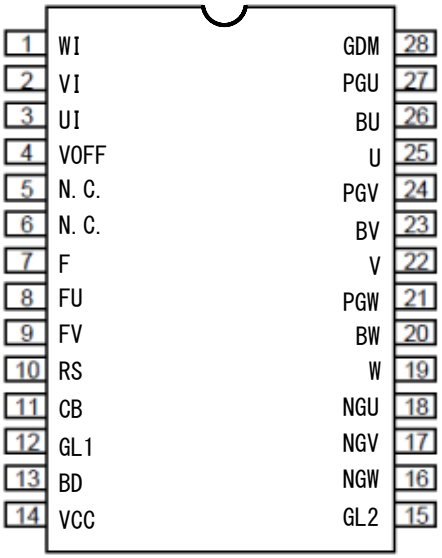


FIGURE 4.1 Pin Locations (Top view)

5. Explanations of Pins

TABLE 5.1 Explanations of Pins

Pin No.	Symbol	Explanation	Remark
1	WI	W-phase control signal input	
2	VI	V-phase control signal input	
3	UI	U-phase control signal input	
4	VOFF	All off signal input	
5	N.C.	No connection	* 2
6	N.C.	No connection	* 2
7	F	Fault signal output	
8	FU	U-phase back EMF signal output	
9	FV	V-phase back EMF signal output	
10	RS	Rs voltage input for over-current detection	
11	CB	VB power supply output	
12	GL1	Control system GND	
13	BD	For bootstrap diode	
14	VCC	15V control power supply	
15	GL2	Reference pin of bottom arm outputs (connected to a current detection resistor)	
16	NGW	W-phase bottom arm gate drive signal output	
17	NGV	V-phase bottom arm gate drive signal output	
18	NGU	U-phase bottom arm gate drive signal output	
19	W	Reference pin of W-phase top arm output	* 1
20	BW	W-phase top arm driving circuit power supply	* 1
21	PGW	W-phase top arm gate drive signal output	* 1
22	V	Reference pin of V-phase top arm output	* 1
23	BV	V-phase top arm driving circuit power supply	* 1
24	PGV	V-phase top arm gate drive signal output	* 1
25	U	Reference pin of U-phase top arm output	* 1
26	BU	U-phase top arm driving circuit power supply	* 1
27	PGU	U-phase top arm gate drive signal output	* 1
28	GDM	Non-usable pin (GND potential. Do not connect anything to this pin.)	

*1. High voltage pin

*2. Not connected to the internal IC chip

6. Inspection

Hundred percent inspection shall be conducted on electric characteristics at room temperature (Ta=25±5℃).

7. Cautions

7.1 Countermeasures against Electrical Static Discharge (ESD)

(a) IC needs to be dealt with caution to protect from damage by ESD. Material of container or any device to carry semiconductor devices should be free from ESD, which may be caused by vibration while transportation. To use electrically conductive container or aluminum sheet is recommended as an effective countermeasure.

(b) What touches semiconductor devices such as work platform, machine and measuring and test equipment should be grounded.

(c) Workers should be grounded connecting with high impedance around 100kΩ to 1MΩ while dealing with semiconductor to avoid damaging IC by electric static discharge.

(d) Friction with other materials such as a high polymer should not be caused.

(e) Attention is necessary so that electric potential will be kept on the same level by short circuit pins when PC board with mounted IC is carried and that vibration or friction might not occur.

(f) The humidity at assembly line to mount IC on circuit boards should be kept around 45 to 75 percents using humidifiers or such. If the humidity cannot be controlled sufficiently, using neutralization apparatus such as ionizers are effective.

7.2 Maximum Ratings

Regardless of changes in external conditions during use, “maximum ratings” should never be exceeded in designing electronic circuits that employ products. In a case maximum ratings are exceeded, products may be damaged or destroyed. In no event shall Hitachi Power Semiconductor Device, Ltd. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the maximum ratings.

7.3 Derating Design

Continuous high-loaded (high temperature, high voltage, large current) operation should be avoided and derating design should be applied, even within the ranges of the maximum ratings, to ensure reliability.

7.4 Safe Design

Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.

7.5 Usage

Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, automobile, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers.

Hitachi Power Semiconductor Device, Ltd. assumes no liability for applications assistance, customer product design, or performance. In such cases it is advised customers to ensure circuit and/or product safety by using semiconductor devices that assures high reliability or by means of user’s fail safe precautions or other arrangement. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

7.6 Soldering

This power semiconductor product is lead-free. The recommended reflow soldering condition is shown in FIGURE 7.1.

7.7 Others

See “Precautions for Use of Hitachi High-Voltage Monolithic ICs” for other precautions and instructions on how to deal with these kinds of products.

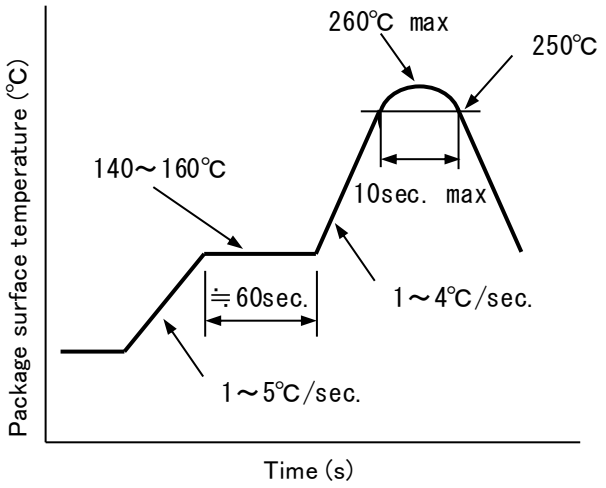


FIGURE 7.1 Recommended Conditions for Infrared Reflow or Air Reflow

8. Important Notices

(1) Hitachi Power Semiconductor Device, Ltd. warrants performance of its power semiconductor products (hereinafter called “products”) to the specifications applicable at the time of sale in accordance with this specification document. Testing and other quality control techniques are utilized to the extent Hitachi Power Semiconductor Device, Ltd. needs to meet specifications described in this specification document. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.

(2) Should any claim be made within one month of product delivery about products’ failure to meet performance described in this specification document, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before of such claim shall not be counted for such response.

(3) Hitachi Power Semiconductor Device, Ltd. assumes no obligation or any way of compensation should any fault about customer’s goods using products be found in marketplace. Only in such a case fault of Hitachi Power Semiconductor Device, Ltd. is evident and products concerned do not meet this specification document, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.

(4) Hitachi Power Semiconductor Device, Ltd. reserves the right to make changes in this specification document and to discontinue mass production of the relevant products without notice. Customers are advised before purchasing to confirm specifications of the product of inquiry is the latest version and that the relevant product is on mass production status in such a case purchasing is suspended for one year or more.

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◆Appendix - Supplementary Data

1. Dimensions

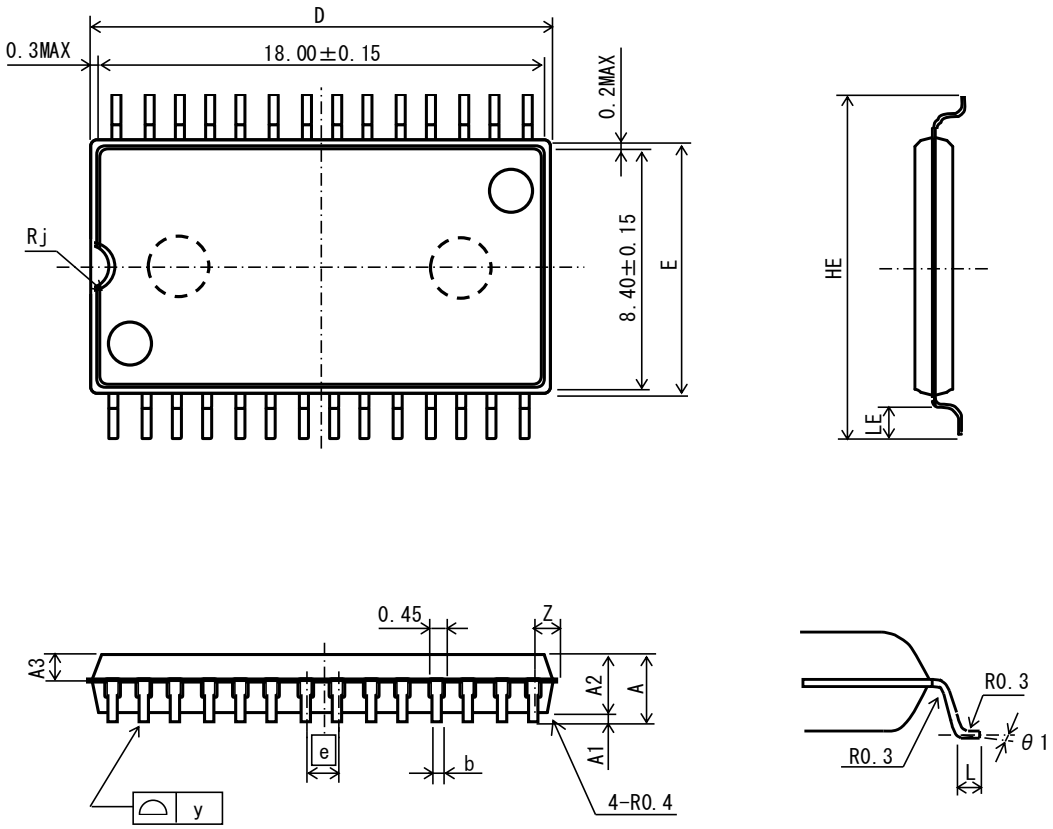

FIGURE 1.1 Dimensions

TABLE 1.1 Dimensions

	MIN	TYP	MAX
A	—	—	2.40
A1	0.10	—	—
A2	—	2.00	2.10
A3	0.75	0.85	0.95
b	0.32	0.40	0.48
D	—	—	18.75
E	—	8.60	8.80
e	1.17	1.27	1.37
HE	11.50	11.80	12.10
L	0.80	1.00	1.20
LE	—	1.70	—
Rj	—	0.60	—
Z	—	—	1.12
θ1	0°	—	8°
y	—	—	0.15

Precautions for Safe Use and Notices

If semiconductor devices are handled in an inappropriate manner, failures may result. For this reason, be sure to read the latest version of “Instructions for Use of Hitachi High-Voltage Monolithic ICs” before use.

This mark indicates an item requiring caution.

CAUTION This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.

CAUTION

(1) Regardless of changes in external conditions during use of semiconductor devices, the “maximum ratings” and “safe operating area(SOA)” should never be exceeded when designing electronic circuits that employ semiconductor devices.

(2) Semiconductor devices may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

(3) If semiconductor devices are applied to uses where high reliability is required, obtain the document of permission from HPSD in advance (Automobile, Train, Vessel, etc.). Do not apply semiconductor devices to uses where extremely high reliability is required (Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.).

(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

NOTICES

1. This Data Sheet contains the specifications, characteristics, etc. concerning power semiconductor products (hereinafter called “products”).
2. All information included in this document such as product data, diagrams, charts, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, specifications of products, etc. are subject to change without prior notice. Before purchasing or using any of the HPSD products listed in this document, please confirm the latest product information with a HPSD sales office.
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7. In no event shall HPSD be liable for any failure in HPSD products or any secondary damage resulting from use at a value exceeding the maximum ratings.

Refer to the following website for the latest information. Contact a HPSD sales office if you have any questions.

http://www.hitachi-power-semiconductor-device.co.jp/en/