# 3-Phase IGBT/MOS Gate Driver IC

# ECN30551FP Product Specifications

Rev.2

#### 1. Product Description

- 1.1 Features
  - (1) PWM control of top and bottom arms is possible with six control signals
  - (2) Free run condition is detected by the built-in back EMF\* detection circuit
  - (3) Maximum Ratings: 620V, suitable for the system from 200VAC to 240VAC
  - (4) Drives a motor using a high voltage DC power supply and a low voltage DC power supply (15V)

#### 1.2 Functions

- (1) Six input type
- (2) FU and FV signal output pins for U and V-phase back EMF detection
- (3) Fault output pin
- (4) Built-in bootstrap diode
- (5) 5V power supply
- (6) Over-current protection
- (7) 15V\_VCC low-voltage detection
- (8) Top arm low-voltage detection

\*EMF: Electromotive Force

## 1.3 Block Diagram

The ECN30551 is shown inside the bold line.

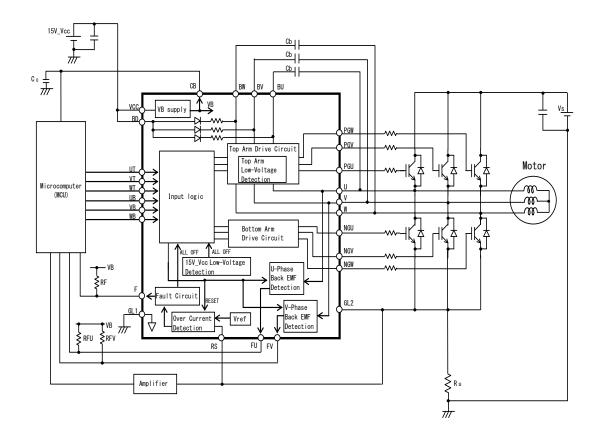
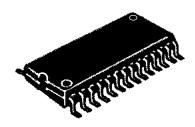


FIGURE 1.3.1 Block Diagram

## 1.4 Packages



ECN30551FP (Package: SOP-28)

FIGURE 1.4.1 Packages of ECN30551FP

## 2. Specification

## 2.1 Maximum ratings

TAB	TABLE 2.1.1 Maximum ratings Condition: Ta=25°C							
No.	Item	Symbol	Pin	Rating	Unit	Condition		
1	High voltage device breakdown voltage	VBV	BU,BV,BW	620	V			
2	GL2 pin voltage	VGL2	GL2	-5 to VCC	V			
3	U, V, W pin voltage	VU,VV,VW	U,V,W	-5 to 600	V			
4	Voltage between BU-BD, BV-BD, BW-BD	VBUD VBVD VBWD	BU,BV,BW, BD	-5 to 600	V			
5	VCC power supply voltage	15V_VCC	VCC	20	V			
6	Voltage between BU-U, BV-V, BW-W	VBSU VBSV VBSW	BU,U BV,V BW,W	20	٧			
7	Voltage between VCC-GL2	VCCGL2	VCC,GL2	23	V	-5V≦VGL2≦-3V		
8	Input voltage	VIN	UI,VI,WI VOFF,RS	-0.5 to VB+0.5	V			
9	Fault pin voltage	Vflt	F	-0.5 to VB+0.5	V			
10	FU, FV pin voltage	Vfu,Vfv	FU,FV	-0.5 to VB+0.5	V			
11	VB supply output current	IBMAX	СВ	50	mΑ			
12	Operating Junction temperature	Tjop	_	-40 to +125	°C			
13	Storage temperature	Tstg	_	-40 to +150	Ĵ			

### Note 1: Thermal resistance

Between junction and air (Mounted PCB\*) : 96°C/W [Reference value]

(Material of PCB : Glass epoxy, PCB size : 40mm × 40mm × 1.6mm, Wiring density : 10%)

\*PCB: Printed Circuit Board

### 2.2 Electrical Characteristics

TABLE 2.2.1 Electrical Characteristics Suffix (T: Top arm, B: Bottom arm), b/w: between Condition: Ta=25°C

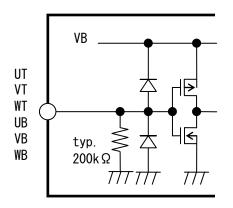
_	ABLE 2.2	1 Electrical Char	acteristics	Suffix (T: Top arm, B: Bottom arm), b/w: betw		betweer				
No.		Item	Symbol	Pin	Min.	Тур.	Max.	Unit	Condition	
1	Standby	current	ls1	VCC	_	3	10	mA	VCC=15V, GL2=0V	
									VOFF=0V, IB=0A	
			ls2	BU,BV,BW	_	15	30	μΑ	Between BU-U,BV-V,BW	/-W=15V
2	Output so	urce current	lo+	PGU,PGV,PGW	0.20	0.25	_	Α	VCC=15V, Pulse width≦	≦10µs
				NGU,NGV,NGW					Between BU-PGU,BV-P	GV,BW-PGW,
									VCC-NGU,NGV,NGW=15V	
3	Output sir	nk current	lo-	PGU,PGV,PGW	0.30	0.40	_	Α	VCC=15V, Pulse width≦10μs	
				NGU,NGV,NGW					Between PGU-U,PGV-V,PGW-W	
									NGU,NGV,NGW-GL2=15V	
4	High leve	output voltage	VOH	PGU,PGV,PGW	_	_	100	mV	VCC=15V, Io+=0A	
				NGU,NGV,NGW					Between BU-PGU,BV-P	GV,BW-PGW
									Between VCC-NGU,NG	V,NGW
5	Low level	output voltage	VOL	PGU,PGV,PGW	_	_	100	mV	VCC=15V, Io-=0A	
				NGU,NGV,NGW					Between PGU-U,PGV-V	
	_								Between NGU,NGV,NGV	N-GL2
6	Output	Turn ON	TdONT	PGU,PGV,PGW	_	0.4	1.0	μs	VCC=15V, CL=1000pF	
7	delay		TdONB	NGU,NGV,NGW	_	0.4	1.0	μs		
8	time	Turn OFF	TdOFFT	PGU,PGV,PGW	_	0.4	1.0	μs	VCC=15V, CL=1000pF	
9			TdOFFB	NGU,NGV,NGW	_	0.4	1.0	μs		
10	•		IL	BU,BV,BW	_	_	10	μΑ	BU,BV,BW=U,V,W=450V	/
	voltage pin			U,V,W						
11		ent protection	Vref	RS	0.45	0.50	0.55	V	VCC=15V	
10	reference	ent protection				0.0	4.0		\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	
12	delay time		Tref	RS	_	2.0	4.0	μs	VCC=15V, CL=1000pF	
13	UT,VT,W		VIH	UT,VT,WT	2.5	_	_	V	VCC=15V	
14	UB,VB,W		VIL	UB,VB,WB		_	1.0	V	100	
15	inputs	Current	IIL	UT,VT,WT	-10	_	_	μA	Input =0V, VCC=15V	Pull-down
16	•	Gurron	IIH	UB,VB,WB		_	100	μA	Input =4.5V, VCC=15V	resistor
10				, ,			100	μ, τ	mput = 1.00, 000=100	NOTE 1
17	RS input	current	IILRS	RS	-100	_	_	μA	VCC=15V, RS=0V	
									Pull-up resistor NOTE	2
18	VB	Voltage	VB	СВ	4.5	5.0	5.5	V	VCC=15V, IB=0A	
19	supply	Current	IB	СВ	_	_	45	mA	VCC=15V	
	output							, (		
20	LVSD	Operating voltage	LVSDON	vcc	9.5	11.0	12.5	V	NOTE 3	
21		Recovery voltage	LVSDOFF		10.0	11.5	13.0	V		
22	Top arm	Operating voltage	LVSDONT	BU,BV,BW	9.0	10.5	12.0	V		
23	LVSD	Recovery voltage	LVSDOFFT		9.5	11.0	12.5	V		
24	F, FU, FV	output resistance	RON	F,FU,FV	_	0.4	8.0	kΩ	I= −1mA NOTE 4	
25	Fault rese	t delay time	tflrs	F	_	15	30	μs	VCC=15V	
26	Bootstrap	diode forward	VFDB	BU,BV,BW,BD	_	1.0	1.5	V	I=1mA, Between BD-BU	J,BV,BW
	voltage								Included series resistan	ce
27			VIHE	U,V	4	_	_	V	VCC=15V	
28			VILE	]	_	_	1	V	UT,VT,WT,UB,VB,WB=0	V
			-							

Note 1: Internal pull-down resistor is typically  $200k\Omega$ . The equivalent circuit is shown in FIGURE 2.2.1.

Note 2: Internal pull-up resistor is typically  $200k\Omega$ . The equivalent circuit is shown in FIGURE 2.2.2.

Note 3: The LVSD function detects and shuts down at low VCC.

Note 4: The equivalent circuit is shown in FIGURE 2.2.3.



<u>V</u>B typ. typ. 200kΩ ≶ Comparator  $220k\,\Omega$ RS Latch typ. 5pF Reset signal

FIGURE 2.2.1 Equivalent Circuit around UT, VT, WT, UB, VB, WB Pins

FIGURE 2.2.2 Equivalent Circuit around RS Pin

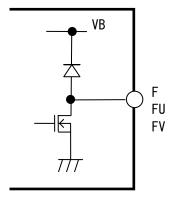


FIGURE 2.2.3 Equivalent Circuit around F, FU, FV Pins

## 2.3 Operating Condition

**TABLE 2.3.1 Operating Condition** 

TAB	TABLE 2.3.1 Operating ConditionCondition: Ta=25°C								
No.	Item	Symbol	Pin	Min.	Тур.	Max.	Unit	Condition	
1	U, V, W voltage	VUVWop	U, V, W	-3	-	450	V	VCC=15V Each voltage between BU-U, BV-V, BW-W: 15V	
2	VCC voltage	VCCop	VCC	13.5	15	16.5	V		
3	Voltage between BU-U, BV-V, BW-W	VBSUop VBSVop VBSVop	BU, U BV, V BW, W	12.0	15	16.5	V		

## 2.4 Functions and Operations

### 2.4.1 Truth Table

**TABLE 2.4.1.1 Truth Table** 

Pin	Input	Output	
UT, VT, WT,	L	L	
UB, VB, WB	Н	Н	
UT, UB	UT=UB=H	PGU=NGU=L	
VT, VB	VT=VB=H	PGV=NGV=L	
WT, WB	WT=WB=H	PGW=NGW=L	

## 2.4.2 Definition of Output Delay Time

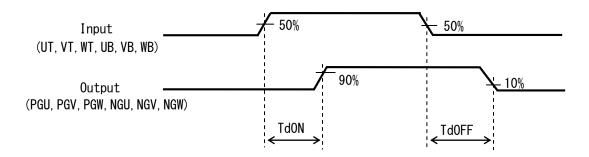


FIGURE 2.4.2.1 Definition of Output Delay Time (Capacitive Load)

#### 2.4.3 Over-Current Protection

The ECN30551 monitors the current through the shunt resistance Rs. When the voltage at the RS pin exceeds the Vref (Typ. 0.5V) of the internal detection circuit, the outputs of the top and bottom arms become all "L" and the F pin outputs "L". Input "L" at all of the UT, VT, WT, UB, VB, and WB pins to reset this "All-Off" state. The F pin outputs "H" by inputting "L" after a lapse of the fault reset delay time (tflrs). Lengthen the period of the six input signals (UT, VT, WT, UB, VB, WB) "L" for the fault reset delay time or more.

Just after the VCC power supply is turned on, the over current protection may operate. In this case, reset the "All-Off" state.

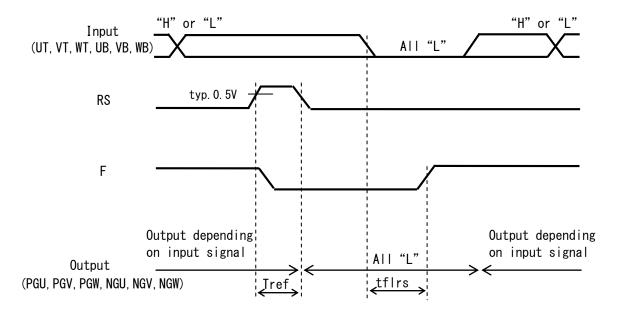


FIGURE 2.4.3.1 Definition of Tref and tflrs

#### 2.4.4 15V\_VCC Low-Voltage Detection

When the 15V\_VCC voltage goes below the LVSD operating voltage (LVSDON), the outputs of the top and bottom arms become all "L". When the 15V\_VCC voltage goes up, this all "L" state is reset at the LVSD recovery voltage (LVSDOFF).

#### 2.4.5 Top Arm Low-Voltage Detection

When the voltage between BU and U (BV and V, or BW and W) goes below the top arm low-voltage detection operating voltage (LVSDONT), the top arm output of the corresponding phase becomes "L". The "L" output state is reset when the "H" signal is input to the top arm after the voltage between BU and U (BV and V, or BW and W) goes up to the top arm low-voltage detection recovery voltage (LVSDOFFT).

## 3. Standard Applications

## 3.1 External Components

**TABLE 3.1.1 External Components** 

Component	Standard value	Usage	Remark
C0	1.0μF ± 20%	Smooths the internal power supply (VB)	Voltage stress is VB (=5.5V)
Cb	$3.3\mu F \pm 20\%$	For bootstrap	Voltage stress is 15V_VCC
Rs	Note 1	Sets over-current protection	
RF, RFU, RFV	10kΩ±5%	Pull-up resistor	

Note 1. The over-current detection setting IO is calculated as follows. IO = Vref / Rs (A)

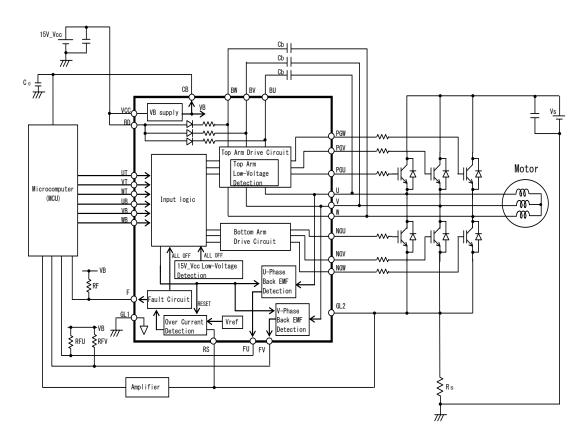


FIGURE 3.1.1 Block Diagram (ECN30551 is shown inside the bold line.)

# 3.2 Input Pins (UT, VT, WT, UB, VB, WB)

In some applications, input pins may be sensitive to noise due to high impedance. If noise is detected at an input pin, the following resistor and/or capacitor should be added.

- Resistor : 5.6k $\Omega$  ± 5% pull-down resistor between the GL pin and input pins
- Capacitor : 470pF ± 20% ceramic capacitor close to the input pins

### 4. Pin Locations

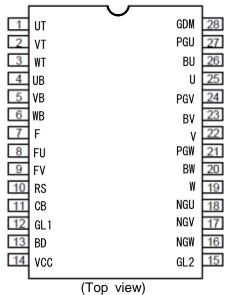


FIGURE 4.1 Pin Locations

# 5. Explanations of Pins TABLE 5.1 Explanations of Pins

Pin No.	Symbol	Explanation	Remark
1	UT	U-phase top arm control signal input	
2	VT	V-phase top arm control signal input	
3	WT	W-phase top arm control signal input	
4	UB	U-phase bottom arm control signal input	
5	VB	V-phase bottom arm control signal input	
6	WB	W-phase bottom arm control signal input	
7	F	Fault signal output	
8	FU	U-phase back EMF signal output	
9	FV	V-phase back EMF signal output	
10	RS	Rs voltage input for over-current detection	
11	СВ	VB power supply output	
12	GL1	Control system GND	
13	BD	For bootstrap diode	
14	VCC	15V control power supply	
15	GL2	Reference pin of bottom arm outputs (connected to a current detection resistor)	
16	NGW	W-phase bottom arm gate drive signal output	
17	NGV	V-phase bottom arm gate drive signal output	
18	NGU	U-phase bottom arm gate drive signal output	
19	W	Reference pin of W-phase top arm output	* 1
20	BW	W-phase top arm driving circuit power supply	* 1
21	PGW	W-phase top arm gate drive signal output	* 1
22	V	Reference pin of V-phase top arm output	* 1
23	BV	V-phase top arm driving circuit power supply	* 1
24	PGV	V-phase top arm gate drive signal output	* 1
25	U	Reference pin of U-phase top arm output	* 1
26	BU	U-phase top arm driving circuit power supply	* 1
27	PGU	U-phase top arm gate drive signal output	* 1
28	GDM	Non-usable pin (GND potential. Do not connect anything to this pin.)	

Note 1. High voltage pin

#### 6. Inspection

Hundred percent inspections shall be conducted on electric characteristics at room temperature  $(Ta=25\pm5^{\circ}C)$ .

#### 7. Cautions

- 7.1 Countermeasures against Electrostatic Discharge (ESD)
  - (a) Customers need to take precautions to protect ICs from electrostatic discharge (ESD). The material of the container or any other device used to carry ICs should be free from ESD, which can be caused by vibration during transportation. Use of electrically conductive containers is recommended as an effective countermeasure.
  - (b) Everything that touches ICs, such as the work platform, machine, measuring equipment, and test equipment, should be grounded.
  - (c) Workers should be high-impedance grounded ( $100k\Omega$  to  $1M\Omega$ ) while working with ICs, to avoid damaging the ICs by ESD.
  - (d) Friction with other materials, such as high polymers, should be avoided.
  - (e) When carrying a PCB with a mounted IC, ensure that the electric potential is maintained at a constant level using the short-circuit terminals and that there is no vibration or friction.
  - (f) The humidity at an assembly line where ICs are mounted on circuit boards should be kept around 45 to 75 percent using humidifiers or such. If the humidity cannot be controlled effectively, using ionized air blowers (ionizers) is effective.

#### 7.2 Storage Conditions

(1) Before opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5°C to 35°C Humidity: 85%RH or lower Period: less than 2 years

(2) After opening the moisture prevention bag (aluminum laminate bag)

Temperature: 5°C to 30°C Humidity: 70%RH or lower Period: less than 1 week

(3) Temporal storage after opening the moisture prevention bag

When ICs are stored temporarily after opening the bag they should be returned into the bag with desiccant within 10 minutes. Then, the open side of the bag should be folded under twice, and closed with adhesive tape. And it should be kept in the following conditions.

Temperature: 5°C to 35°C Humidity: 85%RH or lower Period: less than 1 month

#### 7.3 Maximum ratings

Regardless of changes in external conditions during use of this IC (the product of Hitachi Power Semiconductor Device, hereinafter called "HPSD's IC"), the "maximum ratings" described in this document should never be exceeded when designing electronic circuits that employ HPSD's IC. If maximum ratings are exceeded, HPSD's IC may be damaged or destroyed. In no event shall Hitachi Power Semiconductor Device (hereinafter called "HPSD") be liable for any failure in HPSD's IC or any secondary damage resulting from use at a value exceeding the maximum ratings.

#### 7.4 Derating Design

Continuous high-load operation (high temperatures, high voltages, large currents) should be avoided and derating design should be applied, even within the ranges of the maximum ratings, to ensure reliability.

#### 7.5 Safe Design

The HPSD's IC may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

#### 7.6 Application

If HPSD's IC is applied to the following uses where high reliability is required, obtain the document of permission from HPSD in advance.

· Automobile, Train, Vessel, etc.

Do not apply HPSD's IC to the following uses where extremely high reliability is required.

• Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.

#### 7.7 Soldering

This power semiconductor product is lead-free. The recommended reflow soldering condition is shown in FIGURE 7.7.1.

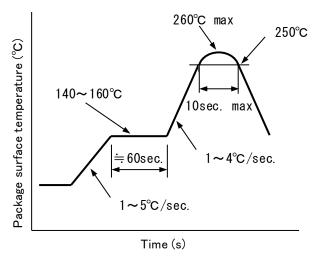


FIGURE 7.7.1 Recommended Conditions for Infrared Reflow or Air Reflow

#### 7.8 Others

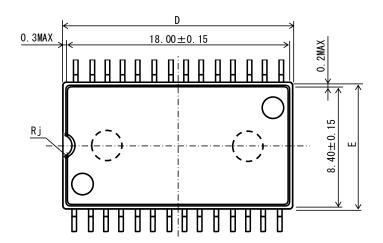
See "Instructions for Use of Hitachi High-Voltage Monolithic ICs" for other precautions and instructions on how to deal with these kinds of products.

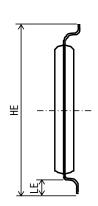
#### 8. Important Notices

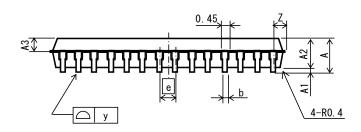
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# ◆Appendix - Supplementary Data

# 1. Dimensions







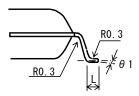


FIGURE 1.1 Dimensions

**TABLE 1.1 Dimensions** 

	MIN	TYP	MAX
Α	_	_	2. 40
A1	0. 10	_	_
A2	_	2. 00	2. 10
A3	0. 75	0. 85	0. 95
b	0. 32	0. 40	0. 48
D	_	-	18. 75
E	_	8. 60	8. 80
е	1. 17	1. 27	1. 37
HE	11.50	11.80	12. 10
L	0.80	1.00	1. 20
LE	_	1. 70	_
Rj	_	0. 60	_
Z	_	_	1. 12
θ1	0°	_	8°
у	_	_	0. 15

## 2. External Packaging

FIGURE 2.1 shows the external packaging. Order quantities are basically multiples of 1000.

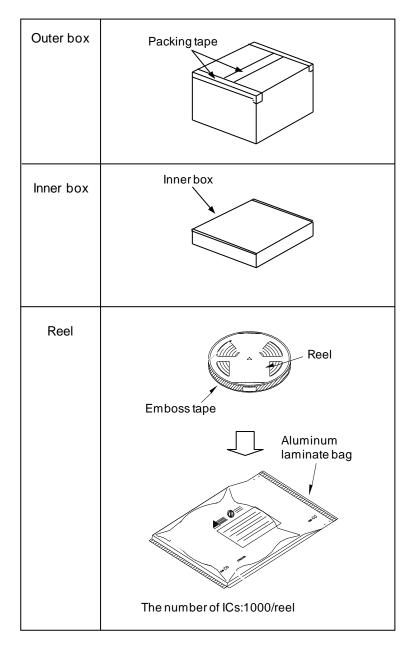


FIGURE 2.1 External packaging

# **Precautions for Safe Use and Notices**

If semiconductor devices are handled in an inappropriate manner, failures may result. For this reason, be sure to read the latest version of "Instructions for Use of Hitachi High-Voltage Monolithic ICs" before use.



This mark indicates an item requiring caution.



**CAUTION** 

This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.



## CAUTION

- (1) Regardless of changes in external conditions during use of semiconductor devices, the "maximum ratings" and "safe operating area(SOA)" should never be exceeded when designing electronic circuits that employ semiconductor devices.
- (2) Semiconductor devices may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.
- (3) If semiconductor devices are applied to uses where high reliability is required, obtain the document of permission from HPSD in advance (Automobile, Train, Vessel, etc.). Do not apply semiconductor devices to uses where extremely high reliability is required (Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.). (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

# **NOTICES**

- 1. This Data Sheet contains the specifications, characteristics, etc. concerning power semiconductor products (hereinafter called "products").
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- 7. In no event shall HPSD be liable for any failure in HPSD products or any secondary damage resulting from use at a value exceeding the maximum ratings.

Refer to the following website for the latest information. Contact a HPSD sales office if you have any questions.

http://www.hitachi-power-semiconductor-device.co.jp/en/